REMARKS

This amendment is submitted in response to the outstanding Office Action, wherein the Examiner rejected Claims 1-38, all the claims under consideration. Reconsideration and allowance of the application in view of the amendments submitted herewith and the following remarks is respectfully requested.

Prior to discussing the rejections of the present Office Action, Applicants take this opportunity to set forth the following brief remarks about their claimed invention. Applicants have discovered that anodizing the dopant regions of a silicon containing substrate produces a high porosity region in proximity to the upper surface of the substrate and a lower porosity region at a greater depth within the substrate, wherein following oxidation of the porous regions the high porosity region coalesces into a Si-containing overlayer and the low porosity region is converted into a buried oxide region, hence forming a silicon-on-insulator substrate. These features are not taught or suggested by the applied prior art.

By this amendment, Claim 1 has been amended to more clearly indicate that the claimed method produces a silicon-on-insulator substrate through anodization of dopant regions to provide differing porosities that contribute to the formation of the buried oxide layer and an SOI layer (also referred to as silicon overlayer) of a silicon on insulator substrate. Claim 1 as amended recites a method of fabricating a silicon-on-insulator substrate that comprises providing a dopant region within a Si-containing substrate; anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region,; and oxidizing said graded porous Si-containing substrate, wherein the first porosity region coalesces to provide a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation. Support for the amendment to Claim 1 is found in paragraphs 0014, 0048, 0058, and original Claims 2 and 37 of Applicants' disclosure. Dependent Claims 2, 3, 4, 7, 12, 13, 14,16, 23, and 24 have been amended to correspond to the amendment to base Claim 1. The subject matter of Claims 15, 25 and 37 have been integrated into the currently amended claims and have therefore been cancelled. Newly added Claim 39 is

supported by original Claim 38. Original Claim 38 is cancelled. The grounds of the rejections in the present Office Action are now discussed in detail.

Claims 1-38 stand rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicants regard as the invention.

In light of the present amendment to the claims, Applicants respectfully submit that the rejections to the term "graded" have been obviated.

Referring to the Examiner's comment that "activating" is a relative term, Applicants respectfully note that definiteness of claim language must be analyzed not in a vacuum, but in light of: (A) The content of the particular application disclosure; (B) The teachings of the prior art; and (C) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. *See* MPEP 2173.02. Applicants submit that the term "activating" as recited throughout the Applicants' specification, e.g. paragraphs 0042-0046, and claimed clearly allows persons of ordinary skill in the art to recognize what is being disclosed. *In re Gosteli,* 872 F.2d 1008, 1012, 10 USPQ2d 1111, 1117 (Fed. Cir. 1989). For example, "activating" is clearly used in context with annealing, wherein annealing is one form of activation that is recognized by one of ordinary skill in the microelectronics art.

Referring to the Examiner's comment that "neutral", as recited in Claims 33-34, is a relative term, Applicants submit that the term has been clearly defined. A fundamental principal of 35 U.S.C. §112, second paragraph, is that the Applicants are their own lexicographers. It is further noted, that any special meaning assigned to a term must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of invention. *See Multiform Desiccants Inc. v. Medzan Ltd.*, 133 F.3d 1350 (Fed. Cir. 1998). With respect to a neutral atom being defined as not interacting with the Si-containing substrate, it would be clear to one of skill in the art that the definition provided in Applicants' disclosure for "neutral atoms" is in reference to chemical interactions, e.g. no chemical interaction, especially when considering the discussion that the neutral atoms can potentially cause physical damage or amorphous regions in the substrate, as described in

paragraph 0022 of Applicants' disclosure. The formation of physical damage and amorphous regions in the substrate result from the physical impact of the neutral ions into the substrate during implantation. Therefore, since the term is definite to one of ordinary skill in the art reading the disclosure, Applicants respectfully request that the rejection be withdrawn.

Turning to the objection to the term "uniform" on Page 3 of the Office Action, Applicants definition was intended to mean what was recited in the specification. Applicants have removed the limitation of "uniform" from the independent claims, wherein the uniform buried oxide is now a feature of amended dependent Claim 23. Hence, the rejection based upon improper claim dependency has been overcome. Therefore, in light of the present amendment, Applicants respectfully request withdrawal of the rejection.

Referring to Page 4 of the Office Action, the Examiner objects to the term "inert gas" as referenced in paragraphs 0044 to 0046 of Applicants' disclosure. It is the Examiner's position that nitrogen is not an inert gas. Applicants note that paragraph 0044 and 0045 recite that a "furnace anneal is typically performed in the presence of an inert gas atmosphere and/or oxidizing ambient, including, for example, He, Ar, O_2, N_2, and mixtures thereof", and that one of ordinary skill in the art reading that passage of the specification in it's entirety would recognize that these gasses are potential constituents of a furnace anneal environment that is suitable for activation steps, regardless of being an inert gas or not. In addition, Applicants observe that the use of N_2 is inert to the Si-containing substrate employed.

Referring to the §112 rejections to dependent Claims 14-17, and 22-26, on pages 4-7 of the Office Action, Applicants have amended dependent Claims 14, 16, 23, 24 to be consistent with newly amended Claim 1, wherein the present amendments have obviated the instant §112 rejection. Additionally, Claims 15 and 25 have been cancelled. Turning to the §112 rejection of Claims 26, Applicants note that amended Claim 1 does not recite the term "uniform"; Claim 26 does not require a single multi-layered silicon on insulator material as alleged by the Examiner; and that Figure 7 of the present disclosure clearly depicts a double SOI that was formed by repeating dopant implantation and oxidation as required by Claim 26. Claim 26 clearly and distinctly recites one aspect of the claimed invention. Therefore, Applicants respectfully request that the §112 rejection to Claim 26 be withdrawn.

Applicants submit that the §112 rejection of Claim 35 has been obviated by the present amendment to Claim 1.

In light of the above, Applicants respectfully request that the 35 U.S.C. §112, second paragraph rejection of Claims 1-38 has been obviated, and respectfully request withdrawal thereof.

The disclosure allegedly stands objected to for minor informalities.

The objection to paragraph 40 stands objected for allegedly having contradictory teachings with respect to the teaching of "a neutral ion that allegedly causes damage formation within the Si-containing substrate", wherein the disclosure teaches that a neutral ion is an ion that does not interact with the Si-containing substrate. As discussed above with respect to the §112 rejection of Claims 33-34, one having ordinary skill in the art reading the disclosure in it's entirety would interpret the definition of the neutral ion to be an ion that does not chemically interact with the Si-containing substrate.

The objection to paragraph 48 has been obviated by the present amendment to the specification.

Applicants respectfully request that the objections to the specification be withdrawn.

Claims 1, 12-14, 16-18, 21, 23-24, (25), 26, 35, and 38 stand rejected, under 35 U.S.C. §102(b), as alleged anticipated by or, in the alternative, under 35 U.S.C. §103(a), as allegedly being unpatentable over JP 09-064323 to Ikeda ("Ikeda"). Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to render Applicants' invention anticipated or obvious, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1.

More specifically, Ikeda fails to teach or suggest a method of fabricating a silicon-on-insulator substrate structure that includes providing a dopant region within a Si-containing substrate; anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate

greater than the first depth, wherein the second porosity region has a lower density that the first porosity region; and oxidizing said first porosity region and second porosity region of the Si-containing substrate, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Consistent with amended Claim 1, paragraphs 0057 and 0058 of Applicants' disclosure state that during the oxidation process the "course porous Si region, i.e., first porosity region, coalesces into monocrystalline Si and then into the Si containing overlayer 22. The thickness of the buried oxide layer and the Si-containing overlayer can be controlled by adjusting the thermal oxidation conditions".

Referring to the abstract and Figure 1 of the Ikeda disclosure, Ikeda discloses a method that includes forming a porous silicon layer 22 by anodic formation and then growing epitaxial silicon on the porous silicon layer 22, wherein the epitaxial silicon provides the SOI layer, i.e. single crystal silicon layer 23. Therefore, since Ikeda requires a separate deposition of epitaxial Si to provide the SOI layer, Ikeda fail to teach or suggest a process in which a first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1.

Further, one would not modify the disclosure of Ikeda to meet the limitations of amended Claim 1, since there is no teaching throughout the Ideka reference of a region having a first porosity and a second porosity of differing density. Referring to page 4 of the Official Action, the Examiner alleges that a silicon substrate with a part thereof turned to a porous layer, is part porous and part not porous, hence may be considered graded with respect to density. Applicants respectfully disagree with this rationale and wish to clarify that the presently amended claims recite a first and second porous region, wherein a part of a substrate that is solid, i.e. not porous, can not meet the limitation of one of the first and second porous regions, as recited in amended Claim 1. Therefore, Ideka also fails to teach or suggest anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, as required by amended Claim 1.

Therefore, since Ikeda fails to teach or suggest at least two required limitations of Applicants' claimed method, as recited in amended Claim 1, Applicants submit that the §102 and §103 rejections of Claims 1, 12-14, 16-18, 21, 23-24, (25), 26, 35, and 38 been obviated and request withdrawal thereof.

Claims 2-11, 15, 19-20, 22, and 29-30 stand rejected under 35 U.S.C. §103(a), as allegedly being unpatentable over JP 09-064323 to Ikeda ("Ikeda") in view of JP 62-245620 to Namito et al. ("Namito et al.") or JP 62-245620 to Ogoto et al. "Ogoto et al.". Applicants respectfully traverse for the following reasons.

Applicants note that Ikeda fail to render Claims 2-11, 15, 19-20, 22, and 29-30 unpatentable, for the same reasons the reference fails to render Claim 1 unpatentable, as recited above. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). To summarize, Ikeda fails to teach or suggest a method of fabricating a silicon-on-insulator substrate structure comprising providing a dopant region within a Si-containing substrate; anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region; and oxidizing said first porosity region and second porosity region of the Si-containing substrate, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1.

Namito et al. also fail to render Applicants' claimed method unpatentable, since Namito et al. also fail to teach or suggest a method of forming a silicon on insulator substrate in which a first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Referring to the abstract and Figure 1 of the Namito et al. reference, Namito et al. disclose a method in which a porous Si region 11 undergoes thermal

oxidation and a Si single crystal 3 is embedded into the porous Si oxide film. In a following process step, amorphous Si is deposited on the porous Si oxide, wherein the single crystal Si 3 acts as a seed to implement single crystal Si growth, i.e. growth of an SOI layer, atop the porous Si oxide film. Therefore, since Namito et al. deposit an SOI layer atop a porous buried oxide layer, Namito et al. does not teach or suggest a method that provides a first porosity region that coalesces into a solid Si-containing overlayer and the second porosity region that is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Further, Namito et al. do not teach or suggest anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, as required by amended Claim 1. Applicants submit that Namito et al. is far removed from the Applicants' invention and note that the Examiner is relying on Namito et al. solely for the teaching of depositing a P-type dopant.

Ogoto et al. fail to fulfill the deficiencies in Namito et al. and Ikeda, because Ogoto et al also fail to teach or suggest a method of forming a silicon on insulator substrate, in which a first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Referring to the abstract and Figure 1 of the Ogoto et al. reference, Ogoto et al. disclose that a "substrate 1 is dipped in a 50% fluoric acid electrolytic solution to render a porous Si film 2. A single crystal Si film is then epitaxially grown on the porous Si film 2' to form an SOI (silicon on insulator) structure." Therefore, since Ogoto et al. deposits an SOI layer atop a porous buried oxide layer, Ogoto et al. does not teach or suggest a method that provides a first porosity region that coalesces into a solid Si-containing overlayer and the second porosity region that is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Further, Ogoto et al. does not teach or suggest anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the substrate porosity region, as required by amended Claim 1.

Applicants submit that the §103 rejection of Claims 2-11, 15, 19-20, 22, and 29-30 citing Ikeda, Ogoto et al., and Namito et al. has been obviated and request withdrawal thereof, since the applied prior art alone or in combination fails to teach or suggest at least two required limitations of Applicants' claimed method, as recited in amended Claim 1.

Claims 1-26, 29-30, 35, 36 and 38 stand rejected under 35 U.S.C. §103(a), as allegedly being unpatentable over US2002/0086463 to Houston et al. ("Houston et al.") in view of Namito et al. or Ogoto et al. Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to render Applicants' invention obvious, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1. Specifically, the applied prior art fails to teach or suggest a method of fabricating a silicon-on-insulator substrate structure comprising providing a dopant region within a Si-containing substrate; anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region; and oxidizing said first porosity region and second porosity region of the Si-containing substrate, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1.

Referring to Paragraphs 0016, 0017 and Figure 1 of the Houston et al. reference, Houston et al. disclose a method of forming a silicon on insulator substrate that includes the steps of providing a porous silicon region in the substrate by boron doping; epitaxial growth of a Si layer atop an the porous silicon surface; and implanting oxygen into the porous layer using a plasma oxygen implant or other oxygen implantation methods, wherein the implanted oxygen provides the buried oxide layer.

Therefore, since Houston et al. deposits an epitaxial Si layer atop a porous silicon region and then implants oxygen to provide a buried oxide layer, Houston et al. does not teach or suggest a method that provides a first porosity region that coalesces into a solid Si-containing

overlayer and the second porosity region that is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Further, Houston et al. does not teach or suggest anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, as required by amended Claim 1.

Applicants note that Namito et al. and Ogoto et al. fail to alleviate the deficiencies in Houston et al., because Namito et al. and Ogoto et al. also fail to teach or suggest a method of forming an SOI that includes providing a first porosity region that coalesces into a solid Si-containing overlayer and the second porosity region that is converted to a buried oxide region of a silicon on insulator structure during oxidation, as discussed above.

Applicants submit that the §103 rejection of Claims 1-26, 29-30, 35, 36 and 38 citing Houston et al., Ogoto et al., and Namito et al. has been obviated and request withdrawal thereof, since the applied prior art alone or in combination fails to teach or suggest at least one required limitation of Applicants' claimed method, as recited in amended Claim1.

Claims 1-26 & 29-38 stand provisionally rejected on the ground of non-statutory obviousness type double patenting as allegedly being unpatentable over claims 1-25 of co-pending U.S. Patent Application 10/674,647.

Applicants have attached a singed PTO/SB/25 (09-04) terminal disclaimer form to obviate the provisional double patenting rejection over co-pending US Application No. 10/674,647.

Claims 1, 12, 14, 16-24, 25, 26, 31-36, and 38 stand rejected, under 35 U.S.C. §102(e), as allegedly anticipated by, or in the alternative, under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 6,800,518 to Bendernagel et al. ("Bendernagel et al."). Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to anticipate or render obvious Applicants' claimed invention, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1. Specifically, the applied prior art fails to teach or suggest a method of fabricating a silicon-on-insulator substrate structure in which a first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1.

Referring to Column 3, lines 40-60, and Figure 1 of the Bendernagel et al. disclosure, Bendernagel et al. discloses a method that includes forming a layer of porous Si in a surface region of a semiconductor wafer 10, forming an epi-Si layer 30 on the layer of porous Si; selectively implanting ions into predetermined areas of the wafer 10 to form implant regions at or near said interface; and annealing the wafer at an elevated temperature which causes transformation of the implant regions, by reaction with the surrounding layer of porous Si, into buried insulating regions 26, and transformation of unimplanted porous Si, by pore coalescence, into buried void planes 27. Referring to Column 3, lines 15-30, and Figure 1, Bendernagel et al. disclose a structure that includes a semiconductor substrate 10; one or more layers of patterned buried insulating regions 26 and void planes 27 located next to each other and atop the semiconductor substrate 10; and a Si over-layer 30 located atop the one or more layers of patterned buried insulating regions 26 and void planes 27.

Therefore, since Bendernagel et al. produce a SOI layer by epitaxial formation, Bendernagel et al. fail to teach or suggest a method that provides a first porosity region that coalesces into a solid Si-containing overlayer and a second porosity region that is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1. Applicants submit that the §102 and §103 rejections of Claims 1, 12, 14, 16-24, 25, 26, 31-36, and 38 has been obviated and request withdrawal thereof.

Claims 1-24, 25, 26, 31-36 stand rejected on the ground of non-statutory obviousness type double patenting as allegedly being unpatentable over claims 1-14 of U.S. Patent No. 6,800,518 to Bendernagel et al. ("Bendernagel et al.").

Applicants have attached a singed PTO/SB/25 (09-04) terminal disclaimer form to obviate the non-statutory obviousness type double patenting over claims 1-14 of U.S. Patent No. 6,800,518 to Bendernagel et al.

Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 stand rejected, under 35 U.S.C. §102(b), as allegedly being anticipated by, or in the alternative, under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 5, 930, 643, to Sadana et al. ("Sadana '643"), wherein U.S. Patent No. 6,222,253 to Sadana et al. (Sadana '253) has been cited as having a substantially equivalent disclosure to Sadana '643. Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to anticipate or render obvious Applicants' claimed invention, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1. The Sadana '643 and Sadana '253 references fail to disclose anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, as recited in amended Claim 1.

Sadana '643 and Sadana '253 disclose a method that includes implanting oxygen ions into a surface of a semiconductor substrate to form a stable buried damaged region in the semiconductor substrate; implanting second ions into the surface of the semiconductor substrate so as to form an amorphous layer adjacent to the stable buried damaged region, wherein the second ions comprise at least one dissimilar ion than the oxygen ions to provide the damaged region, and oxidizing the structure; and optionally, annealing the oxidized structure. There is no disclosure of anodization throughout the Sadana '643 and Sadana '253 references.

Therefore, since Sadana '643 and Sadana '253 fail to disclose anodization, Sadana '643 and Sadana '253 fail to teach or suggest a method that includes anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate is greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, as recited in amended Claim 1.

Applicants submit that the instant §102 and §103 rejections of Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 have been obviated and request withdrawal thereof.

Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 stand rejected, under 35 U.S.C. §102(e), as allegedly being anticipated by U.S. Patent No. 6, 486, 037, to Norcott, et al. ("Norcott et al"). Applicants respectfully traverse for the following reasons.

Norcott et al. is a continuation in part of Sadana '253, which was a divisional of Sadana '546. Applicants submit that the arguments presented above with respect to Sadana '253 and '546 are equally applicable to the rejections citing Norcott, et al.

Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 stand rejected on the ground of nonstatutory obvious type double patenting as allegedly being unpatentable over Claims 1-39 of Norcott, et al.

Applicants have attached a singed PTO/SB/25 (09-04) terminal disclaimer form to obviate the non-statutory obviousness type double patenting over Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 of over claims 1-39 of Norcott et al.

Claims 1-3, 7-8, 10, 12-15, 18, 21-24, 27-28, 31-33, 35-38 stand rejected, under 35 U.S.C. §102(b), as allegedly being anticipated by, or in the alternative, under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 5,387,541, to Hodge et al. ("Hodge et al."). Applicants respectfully traverse for the following reasons.

Applicants submit that the Hodge et al. fail to anticipate, or render obvious, Applicants' invention, since Hodge et al. fail to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1. Specifically, Hodge et al. fail to teach or suggest a method of fabricating a silicon-on-insulator substrate including providing a dopant

region within a Si-containing substrate; anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing susbstrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region; and oxidizing said first porosity region and second porosity region of the Si-containing substrate, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during the oxidizing, as recited in amended Claim 1.

Hodge et al. disclose a process that includes providing a porous silicon layer by anodization (see Figures 1-2, and column 2, line 35, to column 3, line 5, of Hodge et al. reference); ion implantation to produce an amorphous region in the porous Si (see Figures 1 and 2, and column 3, lines 5-35 of the Hodge et al. reference); and annealing to recrystallize the amorphous Si in providing the SOI layer of a silicon on insulator substrate (see Column 3, lines 35-65 of the Hodge et al. reference). Hodge et al. does not teach or suggest anodizing the dopant regions to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as recited in amended Claim 1.

Hodge et al. fail to teach forming an SOI layer during oxidation. Instead, Hodge et al. rely on a recrystallization step to grow an SOI layer from an amorphous Si region, which does not meet the limitation of an oxidation step that provides both the SOI layer and buried oxide layer, as required by amended Claim 1. Although, Hodge et al. disclose embodiments including oxidation steps following and prior to the formation of the SOI layer, in each of the embodiments disclosed Hodge et al. is relying on a separate anneal step in a non-oxidizing environment, i.e., an anneal including argon or nitrogen anneal (see column 3, lines 60-65, of the Hodge et al.), to produce the SOI layer from a recrystallized growth of Si from an amorphous Si region.

Therefore, since Hodge et al. do not disclose forming a porous Si region that includes at least a first and second density portion, and relies on a separate anneal to provide an SOI layer

from recrystallized Si growth, Hodge et al. fail to teach or suggest a method that includes anodizing the dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing structure greater than the first depth, wherein the second porosity region has a lower density that the first porosity region; and oxidizing said first porosity region and second porosity region of the Si-containing substrate, wherein the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during the oxidation, as recited in amended Claim 1.

Applicants submit that the §102 and §103 rejections of Claims 1-3, 7-8, 10, 12-15, 18, 21-24, 27-28, 31-33, 35-38 have been obviated and request withdrawal thereof.

Claims 4-6, 9, 11, 19-20, 25, 26 and 34 stand rejected, under 35 U.S.C. §103(a), as allegedly being obvious over Hodge et al. Applicants respectfully traverse for the following reasons.

Applicants note that Hodge et al. fail to render Claims 4-6, 9, 11, 19-20, 25, 26 and 34 unpatentable, for the same reasons the reference fails to anticipate or render obvious Claim 1, as recited above. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicants submit that the §103 rejections of Claims 4-6, 9, 11, 19-20, 25, 26 and 34 have been obviated and request withdrawal thereof.

Claims 27-28 and 37 stand rejected, on the ground of non-statutory obviousness type double patenting as allegedly being unpatentable over Claims 1-39 of Norcott or Claims 14-38 of Bendernagel et al. in view of Hodge et al.

As discussed above, Applicants have attached singed PTO/SB/25 (09-04) terminal disclaimer forms to obviate the non-statutory obviousness type double patenting over Claims 1-39 of Norcott and Claims 14-38 of Bendernagel et al. Applicants note that Hodge et al. fail to render Claims 27-28 and 37 unpatentable, for the same reasons the reference fails to anticipate or render obvious Claim 1, as recited above. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicants submit that non-statutory obviousness type double patenting rejections of Claims 27-28 and 37 have been obviated and request withdrawal thereof.

Claims 1, 12-14, and 16-17 stand rejected, under 35 U.S.C. §102(b), as allegedly being anticipated by, or in the alternative, under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 5, 023, 200, to Blewer et al. ("Blewer et al."). Applicants respectfully traverse for the following reasons.

Applicants submit that the Blewer et al. fail to anticipate, or render obvious, Applicants' invention, since Hodge et al. fail to teach or suggest each and every limitation of Applicants' claimed method, as recited in amended Claim 1. Blewer et al. is far removed from Applicants' invention as being directed to forming a buried conductive layer in a multi-layered Si substrate. Blewer et al. do not teach or suggest anodizing a dopant region to provide a first porosity region at a first depth of the Si-containing substrate and a second porosity region at a second depth of the Si-containing substrate greater than the first depth, wherein the second porosity region has a lower density that the first porosity region, and then oxidizing first porosity region and second porosity region of the Si-containing substrate, in which the first porosity region coalesces into a solid Si-containing overlayer and the second porosity region is converted to a buried oxide region of a silicon on insulator structure during oxidation, as required by Applicants claimed method recited in amended Claim 1.

Therefore, Applicants submit that the §102 and §103 rejections of Claims 1, 12-14, and 16-17 have been obviated and request withdrawal thereof.

Accordingly, the Examiner is respectfully requested to reconsider the application, withdraw the rejections and issue an immediate a favorable action thereon. If upon review of the application, the Examiner is unable issue an immediate Notice of Allowance, the Examiner is respectfully requested to telephone the undersigned attorney with a view towards resolving any outstanding issues.

An early and favorable action is earnestly solicited.

Respectfully Submitted,

Harry Andrew Hild Jr.
Registration No.: 51,803

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza-Suite 300
Garden City, New York 11530
(516) 742-4343

HAH:tb